ABSTRACT

[0034] A circuit for selectively interconnecting two nodes in an integrated circuit device includes a memory array having a plurality of wordlines and a plurality of bitlines. A refresh transistor has a source coupled to one of the plurality of bitlines, a control gate coupled to a dynamic random access memory wordline and a drain. A switching transistor has a gate coupled to the drain of the refresh transistor, a source coupled to a first one of the nodes and a drain coupled to a second one of the nodes. An address decoder for supplies periodic signals to the wordlines and the dynamic random access memory wordline.